CLAIMS

What is claimed is:

1. In a data processing system with a processor chip that includes a processor core, a store queue (STQ) mechanism with a store queue, and RC dispatch logic, a method for improving gathering capabilities for entries of the store queue that gather processor-issued store operations, said method comprising:

gathering data of a first processor-issued store operation to an entry of the store queue;

activating a timer to track elapsed time from a completion of the gathering step;

when said timer reaches a pre-established threshold for elapsed time, signaling the arbitration logic that said entry is eligible for selection for dispatch to the RC dispatch logic; and

when a second processor-issued store operation gathers to the entry before said pre-established threshold for elapsed time is reached:

holding off tagging said entry as eligible for dispatch; and

restarting said timer to track elapsed time from a completion of said gather of the second processor-issued store operation.

2. The method of Claim 1, further comprising:

monitoring for a receipt of a barrier operation from said processor core; and

when a barrier operation is received,

tagging all active entries as eligible for dispatch; and

preventing further gathering to said active entries, wherein a subsequent store operation targeting a cache line associated with on of said active entries is assigned a new entry within said store queue; and

stopping a respective timer for each active entry.

3. The method of Claim 1, further comprising:

tracking gathers to said entry to determine when said entry contains a full set of store operations to update an entire cache line;

when said contains a full set of store operations, signaling said entry as eligible for dispatch independent of a current status of the timer for that entry, wherein a new gather to said entry does not affect the entry's eligibility for dispatch.

4. The method of Claim 1, further comprising:
monitoring said entry to determining when said entry is still gatherable;
when said entry is no longer gatherable,
signaling said entry as eligible for dispatch; and
stopping said timer for the entry.

5. The method of Claim 4, wherein said timer is a counter that increments each clock tick of a system clock within said data processing system and said threshold for elapsed time is a saturation value of said counter, wherein said counter increment to saturation unless a new gather occurs or said counter is stopped.

6. The method of Claim 5, wherein said STQ mechanism comprises a STQ controller and said counter has an associated counter logic that activates, resets, and stops said counter, wherein said counter logic further signals said STQ controller when said counter has reach said threshold or is stopped.

7. A processor chip for utilization within a data processing system having a memory hierarchy, said processor chip comprising:
a processor core;
a store queue having multiple entries, each having at least an address register and a data register for storing address and data of a store operation issued by the processor core;
a store queue (STQ) controller having an associated arbitration logic, wherein said STQ controller monitors said store queue and identifies when an entry is eligible to be selected for dispatch by the arbitration logic; and
a plurality of timers and an associated timer logic, said plurality of timers being each assigned to an entry and utilized for tracking elapsed time since a last gather of a store operation to that entry; and

logic for signaling an entry as eligible to be selected for dispatch when the timer associated with that entry reaches a pre-established threshold before another store operation gathers into the entry.

8. The processor chip of claim 7, further comprising:

logic for gathering data of a first processor-issued store operation to the entry;

logic for activating the timer to track elapsed time from a completion of the gather of the first processor-issued store operation;

when a second processor-issued store operation gathers to the entry before said pre-established threshold for elapsed time is reached:

logic for holding off tagging said entry as eligible for dispatch; and

logic for restarting said timer to track elapsed time from a completion of said gather of the second processor-issued store operation.

9. The processor chip of Claim 7, further comprising:

logic for monitoring for a receipt of a barrier operation from said processor core; and

when a barrier operation is received,

logic for tagging all active entries as eligible for dispatch; and

logic for preventing further gathering to said active entries, wherein a subsequent store operation targeting a cache line associated with on of said active entries is assigned a new entry within said store queue; and

logic for stopping a respective timer for each active entry.

10. The processor chip of Claim 7, further comprising:

logic for tracking gathers to said entry to determine when said entry contains a full set of store operations to update an entire cache line;

logic that, when said contains a full set of store operations, signals said entry as eligible for dispatch independent of a current status of the timer for that entry, wherein a new gather to said entry does not affect the entry's eligibility for dispatch.

11. The processor chip of Claim 7, further comprising:

logic for monitoring said entry to determining when said entry is still gatherable;

when said entry is no longer gatherable,

logic or signaling said entry as eligible for dispatch; and

logic stopping said timer for the entry.

12. The processor chip of Claim 7, wherein said timer is a counter that increments each clock tick of a system clock within said data processing system and said threshold for elapsed time is a saturation value of said counter, wherein said counter increment to saturation unless a new gather occurs or said counter is stopped.

13. The processor chip of Claim 12, wherein said timer logic that activates, resets, and stops said counter, wherein said timer logic further signals said STQ controller when said counter has reach said threshold or is stopped.

14. The processor chip of Claim 7, further comprising logic that, when said timer reaches a pre-established threshold for elapsed time, said logic signals the arbitration logic that said entry is eligible for selection for dispatch to the RC dispatch logic.

15. A data processing system comprising:

a processor chip that includes:

a processor core;

a store queue having multiple entries, each having at least an address register and a data register for storing address and data of a store operation issued by the processor core;

a store queue (STQ) controller having an associated arbitration logic, wherein said STQ controller monitors said store queue and identifies when an entry is eligible to be selected for dispatch by the arbitration logic; and

a plurality of timers and an associated timer logic, said plurality of timers being each assigned to an entry and utilized for tracking elapsed time since a last gather of a store operation to that entry; and

logic for signaling an entry as eligible to be selected for dispatch when the timer associated with that entry reaches a pre-established threshold before another store operation gathers into the entry; and

a memory hierarchy coupled to said processor chip.

16. The data processing system of claim 15, wherein said processor chip further includes:

logic for gathering data of a first processor-issued store operation to the entry;

logic for activating the timer to track elapsed time from a completion of the gather of the first processor-issued store operation;

when a second processor-issued store operation gathers to the entry before said pre-established threshold for elapsed time is reached:

logic for holding off tagging said entry as eligible for dispatch; and

logic for restarting said timer to track elapsed time from a completion of said gather of the second processor-issued store operation.

17. The data processing system of claim 15, wherein said processor chip further includes:

logic for monitoring for a receipt of a barrier operation from said processor core; and

when a barrier operation is received,

logic for tagging all active entries as eligible for dispatch; and

logic for preventing further gathering to said active entries, wherein a subsequent store operation targeting a cache line associated with on of said active entries is assigned a new entry within said store queue; and

logic for stopping a respective timer for each active entry.

18. The data processing system of claim 15, wherein said processor chip further includes:

logic for tracking gathers to said entry to determine when said entry contains a full set of store operations to update an entire cache line;

logic that, when said contains a full set of store operations, signals said entry as eligible for dispatch independent of a current status of the timer for that entry, wherein a new gather to said entry does not affect the entry's eligibility for dispatch.

19. The data processing system of claim 15, wherein said processor chip further includes:

logic for monitoring said entry to determining when said entry is still gatherable;

when said entry is no longer gatherable,

logic or signaling said entry as eligible for dispatch; and

logic stopping said timer for the entry.

20. The data processing system of claim 15, wherein:

said timer is a counter that increments each clock tick of a system clock within said data processing system and said threshold for elapsed time is a saturation value of said counter, wherein said counter increment to saturation unless a new gather occurs or said counter is stopped; and

said timer logic that activates, resets, and stops said counter, wherein said timer logic further signals said STQ controller when said counter has reach said threshold or is stopped.